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A DVR BUILT WITH A 7 LEVEL CASCADE ASYMMETRIC MULTILEVEL CONVERTER

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ABSTRACT

The power quality (PQ) in distribution systems isprincipally affected by the pollution introduced by the customers. It is necessary to protect the sensitive loads from disturbances such as sags, swells, source voltage imbalances, etc. The actualsolution for this case is to employ a dynamic voltage restorer(DVR) device. The use of multilevel inverters in medium voltageapplications is a good solution. In particular, the cascadedasymmetric multilevel converter (CAMC) appears as a veryattractive alternative among the 7-level converters for thisapplication. The design of the CAMC as a DVR in a mediumvoltage distribution power system is presented in this paper. Themodel and the control strategy are discussed in d-q coordinatessynchronous with the source voltage. The performance of theproposed compensator is tested with SPICE simulations.

Key terms: Asymmetric Multilevel Converters; Dynamic Voltage Restorer (DVR); Unbalanced Voltage Supply; Voltage Sag; Power Quality (PQ).

1. INTRODUCTION

Voltage sags, swells and harmonics are the most frequentdisturbances in the electrical grid, originated by the utilities, theindustrial and the commercial consumers. The disturbancesare caused by motor starting, the connection and disconnectionof large loads, the presence of non-linear loads and in manycases by short-circuits taking place in sub transmission systems. They have an important financial impact and negative effects on industrial equipments. Nowadays, the disturbances arealso important because they can lead to disconnection of largewind farms connected to the grid. All these problemshave found an effective solution with dynamic voltage restorerdevices (DVR).

At low voltage (LV), the DVR is usually implemented with the classical two-level voltage source converter (VSC) via acoupling voltage transformer. In medium voltage (MV) andhigh power applications, the switches of the two-level topologymust block high voltages. Otherwise, a transformer with highturns ratio will be need, increasing both the current in theconverter side and the losses in the DVR. In MV applications Itis more appropriate to implement the DVR with a multilevelvoltage source converter (MVSC). In this way it is possible toreduce the current and losses in the converter.Moreover, it is feasible to combine the action of the DVR witha shunt compensator, sharing the DC bus in a back to backconnection.

In this work, the implementation of the DVR with a cascade asymmetric multilevel converter (CAMC) ispresented. The CAMC is a competitive topology because it haseven voltage levels with a reducednumber of components thanthe classical multilevel converters for medium voltage (MV). The control strategy of the DVR can be designed toexchange either active and reactive powers, or only reactive power. In this work the first approach is adopted because it enhancesthe dynamic range of amplitude and phase of the voltage injected by the DVR compared with the second approach. Taking into account that the principal cause of disturbancesin distribution systems are the short-circuit faults, they areconsidered in order to test the DVR-CAMC. Different faultslike three phase short circuits, one

phase short circuit, in theneighbor load of the sensitive load, are analyzed. They causesymmetric and asymmetric faults at the point of commoncoupling (PCC) along several cycles. The control of the DVR-CAMC has been designed to have fast response to symmetricand asymmetric perturbations at the PCC. The simplest controlsolution consists in a feedback control loop to track the loadvoltage reference, together with a feedforward injection of thePCC voltage to obtain the references for the DVR. In detail, the paper is organized as follow. The distributionpower system, the steady state analysis and control strategy torestore the energy of the DVR-CAMC are presented in SectionII. The description, design and control of the CAMC in asynchronous reference frame are shown in Section IV. Theperformance of the DVR-CAMC together with the controlsystem is tested through simulations with SPICE in Section V.Finally, some conclusions are presented.

2. POWER SYSTEM AND DVR CONTROL STRATEGY

A. Description of the Power System

Figure 1 shows the power system under study, for Disturbance analysis at the PCC in medium voltage level of 13.8 KV. The generator (GS) with LS represents a weak gridwith a short circuit power (Ssc) of approximately 68 MVA. Twosimilar lineal loads of 18 MVA each, with inductive echaracteristics and poor power factor, are connected to thePCC. One load is considered as a sensitive load which must beprotected from the short circuits produced in the neighbor loads. The DVR is connected between the sensitive load andthe PCC through a transformer. The inductor Lf is part of theoutput filter of the CAMC to reduce the voltage ripple due tohigh frequency switching. The DVR is operating with active
power exchange by means of the energy storagesystempresentinDC side of the CAMC. Different types of energy storagesystems can be found in the literature, from batteries to a high temperature superconducting magnetic.

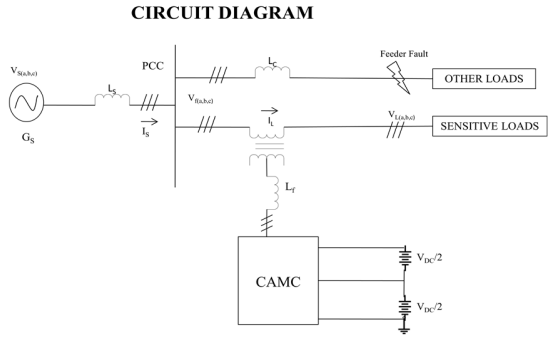


Figure 1: Power system with DVR

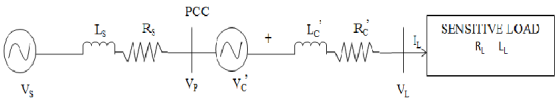


Figure 2: Simplified system

B. Control strategy

The control of the DVR will be designed to regulate the load voltage vL and to compensate sags, swells, and voltageimbalances at the PCC. Figure 2shows a simplified version ofthe one line diagram of the system. The distribution system isrepresented by its voltage generator (vS) and its short circuitimpedance. The DVR is represented by a voltage generator (v'C) with coupling impedance (L'C and R'C). L'C represents thetransformer leakage inductance plus Lf, while R'C representsthe losses of the coupling and the CAMC. The sensitive load ischaracterized by its power consumption and its power factor.

According to Figure 2, the voltage injected in each phase bythe DVR (vDVR) in each phase is,

$$V_{DVR}=V_L-V_P \quad \text{.....(1)}$$

where VL =load voltage
VP =voltage at thePCC.
Ina general case VP can be express as,

$$V_P=V_P^{(1)}+V_P^{(COMP)} \quad \text{.....(2)}$$

BeingVp the positive sequence of the fundamental voltage andVp[comp] represents the negative sequence plus the harmonics.The control strategy tries to keep the load voltage at rated valueeven when different faults occur, so (2) it is re-written as

$$V_{DVR}= V_L^{*}-V_P^{(1)}-V_P^{(COMP)}$$

where V**L** is the load voltage reference.
Considering an harmonics free source voltage, then

$$V_P=V_P^{(1)}+V_P^{(2)}$$

WhereVp= negative sequence voltage
Therefore, the voltage injected by DVR is

$$V_{DVR}= V_{DVR}^{(1)}-V_P^{(2)}$$

Considering an harmonics free source voltage, then

$$V_P=V_P^{(1)}+V_P^{(2)}$$

Where$V_P^{(2)}$is a negative sequence voltage.
Therefore voltage injected by DVR is

$$V_{DVR}= V_{DVR}^{(1)}-V_P^{(2)} \quad \text{.....(3)}$$

Where $V_{DVR}^{(1)} = V_L^* - V_P^{(1)}$

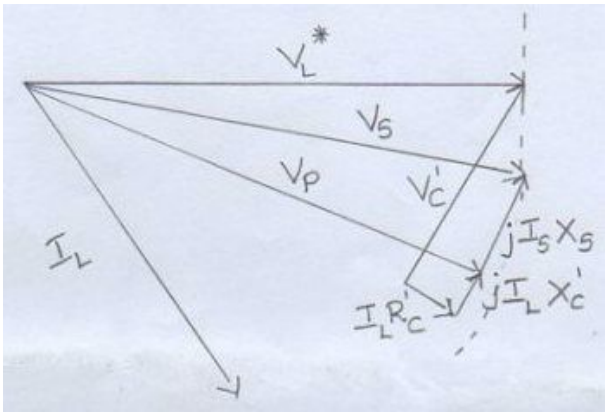


Figure 3 represents the condition of the load voltage regulation by the DVR with disturbances in the PCC.

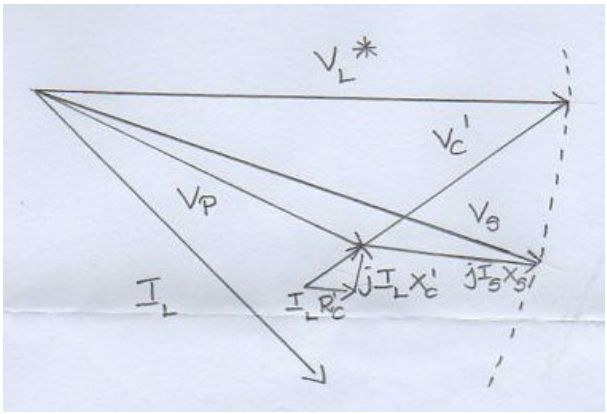


Figure 3 a) represents the condition of the load voltage regulation by the DVR without disturbances in the PCC.

In thiscase VS has the rated value, in consequence the DVRcompensate only the voltage drop in XS, R'C and X'C. Thepower supplied by the source is a little larger than the power consumed by the load since the system supplies only the loadcurrent and VS lags VL. The phase shift between both voltagescan be regulated such that the system can supply the loadpower plus the power loss in R'C (P_{loss}). Then the DVR voltagemust have a 90º phase shift with respect to the load current. If Ploss is very low, the exceeding power provided by thesource must be absorbed by the DVR. So it is possible torecharge the energy storage in the DVR. Therefore in absenceof faults at the PCC, the DVR can recover the energy lostduring sag compensation. Figure 4 shows the diagram of thiscondition

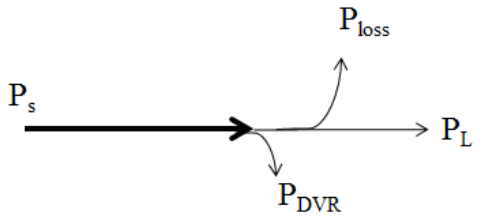


Figure 4: Power flux from source to load and recover of energy to DVR,

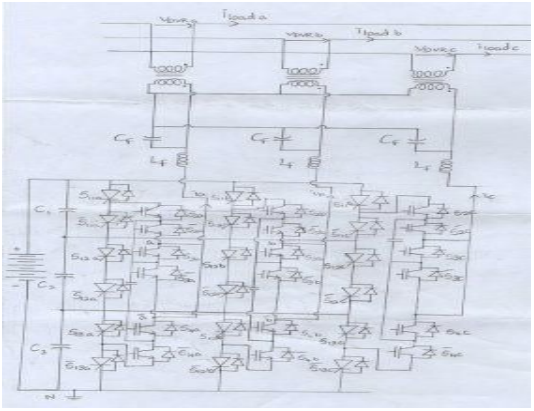


Figure 5 shows a three phase CAMC connected to the system as a DVR.

Voltage sag at the PCC caused by a short circuit is shownin Figure 3 b). The source current is greater than the loadcurrent, so the voltage drop in XS is increased with respect tothe previous condition. Therefore the voltage injected by theDVR must compensate the sag and the drop in R'C and X'C. Itcan be seen that V'C has a leading phase with respect to I_L,supplying active and reactive power to the load

3. CAMC AND CONTROL

A. Cascade Asymmetric Multilevel Converter (CAMC)

Figure 5 shows a three phase CAMC connected to the system as a DVR. Each leg of the converter has one high voltage stage (HV) and one low voltage stage (LV). The HVstage is formed by the switches S1(1,2)i-S1(1,2)i (with i = a,b,c).They are controlled at the modulating frequency with only oneswitching function s1i. The LV stage is a three level flyingcapacitor topology and it is formed by two pairs ofcomplementary switches S2i- S2 i , S3i- S3 i and the capacitor C3i.These switches are controlled by the switching functions s2i ands3i. They are obtained with a pulse width modulation strategyemploying phase shifted carriers (PSC-PWM). This structuretogether with a hybrid modulation strategy allows obtaining 5voltage levels. The hybrid modulator is shown in Figure 6where m(a,b,c) are the modulating signal.

They are inputs to thezero-crossing detectors (ZD) which generate the square waveswitching function (s1(a,b,c)) for the HV stages.

Simultaneously m(a,b,c) are subtracted from the outputs ofthe ZDs to obtain the reference signals to the modulator PSC-PWM. When the modulating signal is a sinusoidal wave form,the reference signal result

$V_{mi}=2.M_i.A_P.\sin(\omega t - \varphi)-A_p.(2S_{1i}-1)$…….(4)

where $0 \leq Mi \leq 1$ is the modulation index, A_P is the amplitudeof the carrier signals and $S_{1i}$is the relative phase of eachmodulating signal applied to each leg of the converter. Assuming a balance system and Therefore the output signals of thepulse width modulator are the switching function s2(a,b,c) ands3(a,b,c) which controls the LV stages.

While $Mi \leq 1$, the fundamental components of the phase

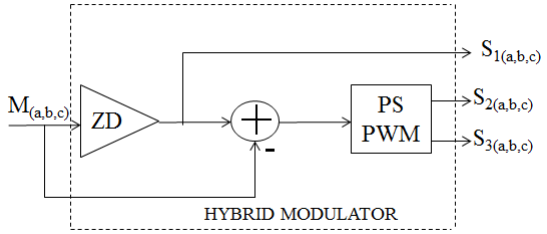


Figure 6: Hybrid modulator for each phase of the CAMC

$V_{iN}= \frac{V_{DC}}{}S_{1i} + \frac{V_{DC}}{}(S_{2i+} S_{3i})$……..(5)

So the three phase fundamental components results as follow,

V_o

$V_o = \frac{V_{DC}}{}$.

V_o

Where

$m_a=M_a.\sin\ \omega t.\varphi$

$m_b=M_b.\sin\ \omega t.\varphi$

$m_c=M_c.\sin\ \omega t.\varphi$

B. CAMC design

The first consideration to design the CAMC is the value ofthe DC voltage. The CAMC requires a high DC voltage toreduce the current on the power switches and also to reduce thelosses. On other hand, a high DC voltage gives the possibility to connect back to back with another CAMC in shuntcompensation without a transformer. Secondly, the flyingcapacitors are designed to carry the DVR rated current with avoltage ripple below 5% of the rated capacitor voltage.

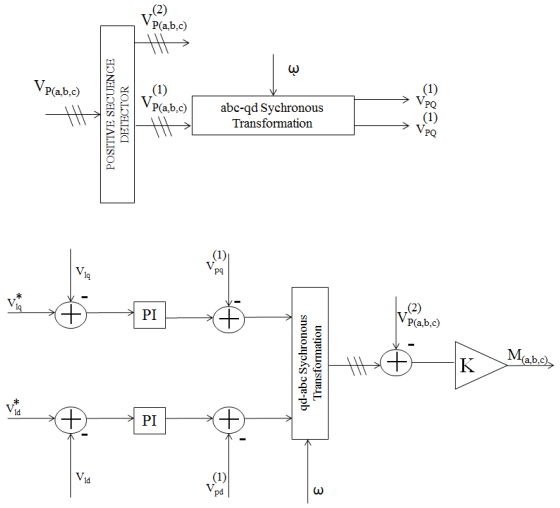


Figure 7: Block diagram of control for DVR

1) Output filter :The output voltage of the CAMC (before the coupling transformer) is filtered by an LC-filter (Lf, Cf) with two goals: to reduce losses in the transformer and to reduce the disturbances at the switching frequency on the acsystem. The values of Lf and Cf were selected to have anegligible voltage drop on Lf and a negligible shunt current throughCf at the fundamental frequency.

2) Voltage Transformer:The design of the transformer is acritical point to define the behavior of the DVR. A poor coupling factor in the transformer introduces a high leakage inductance. This affects the voltage injected by the DVR whenit tries to compensate a voltage imbalance present in the PCC.The transformer ratio was adopted equal to 1:1.5. This designgives an appropriate modulation index of the CAMC whenvoltage sag is present at the PCC. In addition, the leakageinductance of the transformer is low enough. Table Isummarizes the values of the main parameters of the DVR.

C. Control scheme of the DVR

The control scheme in synchronous coordinates is shown inFigure 7. The block diagram of the DVR control has threeparts. The first one consists in the voltage measure at the PCCand the detection of the positive and negative sequences(V p(1)a ,b , c) and V p(2) ,b , c) , respectively). This is followed by the((a abc-qdtransformation of the positive sequence (v (1) and v (1)).pdpqThe second part is the feedback control on the load voltage,regulated by a proportional-integral (PI) control [13]. Thepositive sequence of the first stage is feed forwarded to thecontrol loop. This is

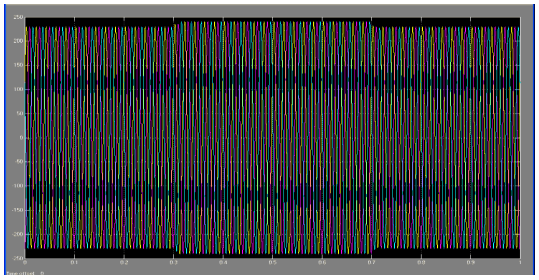
subtracted from the output of the PI. Whenboth the positive sequence and PI output are equal, the voltageinjected by DVR is zero. In the last stage the negative-sequenceis subtracted to balance the voltage on the load. So, themodulation signals for the CAMC are obtained.

4. SIMULATION RESULT

The MV three wires power systems with two linear loads
connected to the PCC (Figure 1) was implemented in Pspicesimulator. Different types of short circuits in the neighborhoodof the sensitive load are tested and analyzed in this section.

A. Three phase short circuit.

In this case the short circuit is a simultaneous three phase fault to ground. The currents wave forms are shown in Figure8: source current (top) and the load current (bottom). Figure 9shows the source voltage (top), load voltage (middle) and DVRvoltage (bottom). It is clearly seen that the DVR is regulatingthe load voltage before the fault occurs. At t = 200ms the shortcircuit occurs and the source current increase to 10 KA per phase. The value of the short circuit current is limited by theinductive impedance of the connection. Moreover, theseimpedances forced a voltage drop at the PCC, falling to near50% of rated value. The DVR injects the appropriated voltageto compensate the sag and keep the voltage on the sensitive load at rated value. At t = 315ms, the fault is disconnected, thevoltage at the PCC restores its operating value and the DVRreduces the voltage to continue regulating the load voltage.



The current (iC) is shown in thetop trace and the phase voltage (vC) in the bottom figure. It isclearly seen the relationship between i_C and the load current(iload_c) through the transformer ratio. The bottom picture showsthe three voltages v_C, v_{DVR} and vload in the phase c of thesystem. The CAMC compensates the voltage drop in XS, R'Cand X'C before the fault (Figure 3 a)). After the fault thevoltage in the PCC falls. So, it can be seen as the CAMCincreases the voltage to keep the rate voltage value in the load

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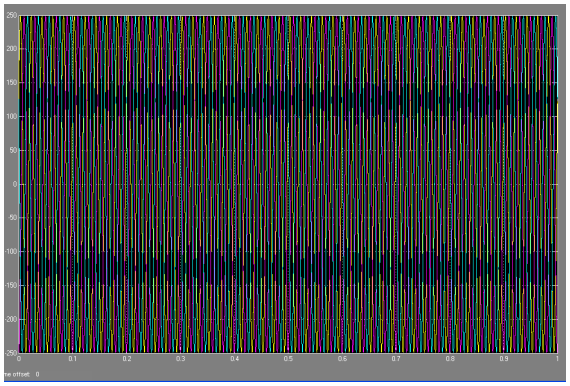
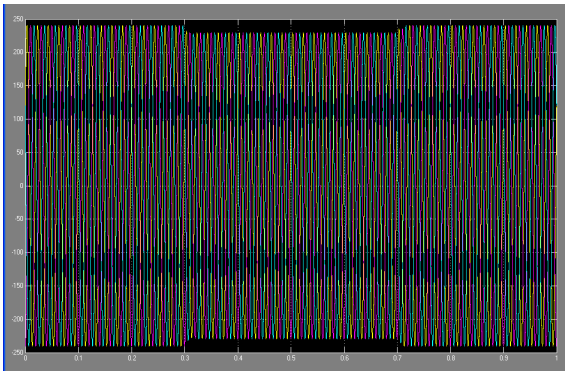


B. Bi-phase short circuit

The bi-phase short circuit is considered when only two phases fault to ground.The voltage on the sensitive load and the injected DVR voltage. The DVR is regulating the sensitive load voltage until t = 200ms when thefault happens and the currents, in the two phases, increase tonear 10 KA. The sag is present only in two phases causingunbalanced voltage in the PCC. While one phase keeps thevoltage value, the voltages in the other two phases fall to 50 %of rated value. The DVR compensates this sag, injectingdifferent voltages on each phase and keeping the sensitive loadvoltage balanced and at the rated value. This condition isstopped at t = 315ms, when the short circuit is isolated and theDVR returns to the regulating condition.

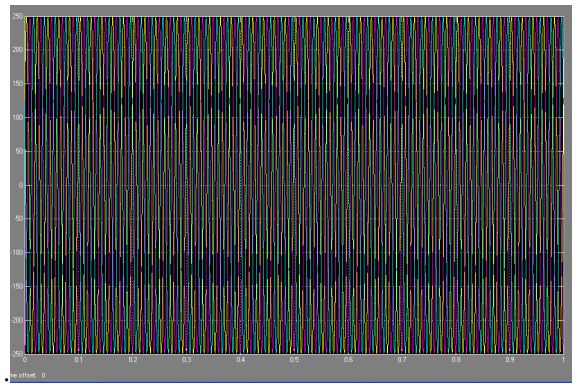
C. Single phase short circuit

Like in the previous cases, theDVR is regulating the voltage before the short circuit happens.At t = 200ms the fault occurs and the current increases to near10KA. This can be seen in the fault load and source current. The fault iscleared at t = 255mesc but the other two phases are interruptedafterwards at t = 310ms. The voltages in the PCC have sag inone phase while the short circuit is present So, while only twophases are connected to the PCC (between 255ms to 310ms),there is a little swell voltage in one phase. It can be seen, that thecontrol action of the DVR keeps the rated voltage in the sensitive load, at every moment.



The control of the DVR corrects this unbalance injecting theappropriated voltage and shift phase, so the voltage on thesensitive load maintains the rated value.

In all the previous tests the DVR is regulating the load voltage before and after the different faults occur. It can be seen that after the fault the DVR voltage has lower value thanbefore the fault. This is so, because the fault load is cleared andthe drop in the source impedance is reduced. Then the voltage injected by DVR is reduced too.



5. CONCLUSIONS

In this work a DVR with a CAMC was designed and testedto see the behavior of the DVR with different disturbances inthe grid. The CAMC is a multilevel converter that offers agood and simple alternative to build a 7-level converter for thisapplication. The control strategy of the DVR was designed toregulate the load voltage and compensate sag, swell, andvoltage unbalances. For this objective the control of the DVR-CAMC employ a simple solution. It has a feed forward actionof the source voltage and a feedback control loop to regulate the load voltage. It has been considered that the most common disturbancesin distribution systems are short circuits. Therefore, symmetricand asymmetric faults, on one load connected to the PCC weretested and analyzed. The performance of the DVR-CAMC wastested through simulations with SPICE. It proves that thecontrol scheme provides an accurate tracking of the voltagereferences and a fast transient response to sag, swell andvoltage unbalances. Finally, it should be noted that it probesthe capability of the proposed DVR-CAMC to work over awide range of operating conditions.

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